Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A dynamic random access memory (DRAM) with a plurality of memory banks comprising:
a pair of separate flag bit registers for each bank with the flag bit registers being shifted up/down respectively,
a comparator for each bank which provides a comparator output,
an arbiter for each bank connected to receive a flag bit up signal and a flag bit down signal from the flag bit registers for that bank and the comparator output from the comparator for that bank,
the arbiters being connected to receive a conflict in signal and to provide a conflict out signal, and
the pair of flag bit registers representing a refresh status of each bank and designating memory banks or arrays that are ready for a refresh operation.

[c2] The DRAM of claim 1 wherein the comparators compare a refresh bank address with an incoming normal access bank address and sends the comparator output result to a conflict signal generator to which all arbiters are connected.

[c3] The DRAM of claim 1 wherein the arbiter coordinates re-

fresh bank activation by combining comparator results and refresh bank activation priority schedule.

[c4] The DRAM of claim 2 wherein the arbiter coordinates refresh bank activation by combining comparator results and refresh bank activation priority schedule.

[c5] The DRAM of claim 1 wherein a row address counter (RAC) for each bank keeps the refresh history of each bank and generates a row address to be refreshed.

[c6] The DRAM of claim 1 wherein memory access sequencing means provides a sequence of refresh operations.

[c7] A dynamic random access memory (DRAM) with a plurality of memory banks including a refresh scheduler book unit comprising:
a pair of separate flag bit registers for each bank with the flag bit registers being shifted up/down respectively,
a comparator for each bank which provides a comparator output,
an arbiter for each bank connected to receive a flag bit up signal and a flag bit down signal from the flag bit registers for that bank and the comparator output from the comparator for that bank,
the arbiters being connected to receive a conflict in signal and to provide a conflict out signal, and

the pair of flag bit registers representing a refresh status of each bank and designating memory banks or arrays that are ready for a refresh operation.

[c8] The DRAM of claim 7 wherein the comparators compare a refresh bank address with an incoming normal access bank address and sends the comparator output result to a conflict signal generator to which all arbiters are connected.

[c9] The DRAM of claim 7 wherein the arbiter coordinates refresh bank activation by combining comparator results and refresh bank activation priority schedule.

[c10] The DRAM of claim 8 wherein the arbiter coordinates refresh bank activation by combining comparator results and refresh bank activation priority schedule.

[c11] The DRAM of claim 7 wherein a row address counter (RAC) for each bank keeps the refresh history of each bank and generates a row address to be refreshed.

[c12] The DRAM of claim 7 wherein components comprising the refresh scheduler book unit are distributed within each bank and communicates through a conflict signal generator that is connected to the comparator and the arbiter.

[c13] The DRAM of claim 7 wherein components comprising the refresh scheduler book unit are isolated from each bank and the refresh scheduler book unit sends to each bank both of a selected refresh bank address and refresh row address kept by row address counter.

[c14] The DRAM of claim 7 wherein all components except row address counter (RAC) are isolated from each bank or array and send to each bank or array a selected refresh bank address.

[c15] The DRAM of claim 7 wherein memory access sequencing means provides a sequence of refresh operations.

[c16] A dynamic random access memory (DRAM) with a plurality of memory banks including a refresh scheduler book unit comprising:
a pair of separate flag bit registers for each bank with the flag bit registers being shifted up/down respectively,
a comparator for each bank which provides a comparator output,
an arbiter for each bank connected to receive a flag bit up signal and a flag bit down signal from the flag bit registers for that bank and the comparator output from the comparator for that bank,
the arbiters being connected to receive a conflict in signal and to provide a conflict out signal, and

the pair of flag bit registers representing a refresh status of each bank and designating memory banks or arrays that are ready for a refresh operation,
memory access sequencing means for providing a sequence of refresh operations, and
a conflict signal generator included in each of said arbiters.

[c17] The DRAM of claim 16 wherein the arbiter coordinates refresh bank activation by combining comparator results and refresh bank activation priority schedule.

[c18] The DRAM of claim 16 wherein a row address counter (RAC) for each bank keeps the refresh history of each bank and generates a row address to be refreshed.

[c19] The DRAM of claim 16 wherein components comprising the refresh scheduler book unit are isolated from each bank and the refresh scheduler book unit sends to each bank both of a selected refresh bank address and refresh row address kept by row address counter.

[c20] The DRAM of claim 16 wherein all components except row address counter (RAC) are isolated from each bank or array and send to each bank or array a selected refresh bank address.